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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,771	12/24/2003	Yasuo Inoue	57454-981	9456

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,771	INOUE ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/264,116.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Preliminary Amendment filed on December 24, 2003.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 34, 35, and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by Kumagi (US 5,397,906).

In re claim 34, Kumagi shows (figs. 5A-5C) a semiconductor layer (1') arranged on a main surface of a semiconductor substrate (1) with an insulating layer (14) between said semiconductor substrate and said semiconductor layer, a plurality of MOS field effect transistors (6) of a first conductivity type at a first active region (Q_N) of said semiconductor layer, and an MOS field effect transistor (3) of a second conductivity type

at a second active region (Q_P) of said semiconductor layer. Kumagi shows in figure 5C that said first active region comprises a first isolation region including a first insulating layer (FOX region 13 between adjacent transistors 6), said plurality of MOS field effect transistors of the first conductivity type being isolated from each other by said first isolation region. A second isolation region including a second insulating film (FOX region 13 separating regions Q_N and Q_P) is provided between said first active region and said second active region, and said first active region and said second active region being electrically isolated from each other by said second isolation region.

In re claim 35, Kumagi shows (fig. 5C) a lower semiconductor layer (portion of P^-) remains under said first insulating film in said first isolation region, each portion of said semiconductor layer provided in said first active region being electrically connected with each other integrally by said lower semiconductor layer.

In re claim 45, Kumagi shows (fig. 5A-5C) an electrode (Vcc or GND) is provided in respective said semiconductor layer of said first active region and said second active region, and said electrode is held at a ground potential or a predetermined fixed potential.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumagi (US 5,397,906) as applied to claims 34 and 35 above, and further in view of Ogoh (US 5,436,482).

In re claim 36, Kumagi shows all of the elements of the claims except the field shield gate electrode provided above the first insulating layer, which Ogoh discloses (col. 11, lines 55-64). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the isolation region of Kumagi by adding a field shield gate electrode as taught by Ogoh to provide additional isolation of active regions.

In re claim 37, Ogoh also discloses (col. 11, lines 55-65) that the insulating film in the first isolation region is an oxide film made by local oxidation of said semiconductor layer. However, such a limitation is a "product by process" limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17**(footnote 3). See also in re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116** in re Wertheim, **191 USPQ 90** (**209 USPQ 254** does not deal with this issue); and In re Marosi et al, **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear. "Even though product-by- process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a

product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

Claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumagi (US 5,397,906) as applied to claims 34 and 35 above, and further in view of Nagakubo et al. (US 4,478,655).

In re claims 38 and 39, Kumagi shows all of the elements of the claims except the second insulating film in said second isolation region is a replacement for said semiconductor layer in said second isolation region completely removed or that the second isolation region is an oxidation of all said semiconductor layer in said second isolation region. Nagakubo et al. shows (fig. 6) a semiconductor layer (132) formed on an insulating substrate (131). The active regions of the layer are isolated and divided by an insulating film 110 that is a replacement for the semiconductor layer. The semiconductor layer is completely removed in that the insulating film is an oxidation of all of the semiconductor layer. With this configuration, the active layers can be completely separated into island substrate regions (col. 11, lines 20-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second isolation region of Kumagi by forming the insulating film completely through the semiconductor layer as taught by Nagakubo to completely separate the active layers into island substrate regions.

In re claim 40, Nagakubo shows (fig. 6) that a portion of said second insulating film in said second isolation film (110) is an insulating film identical to an interlayer insulating film (121) provided above said MOS field effect transistor of the first conductivity type or said MOS field effect transistor of the second conductivity type. The isolation film and interlayer insulating film are both made of silicon oxide.

Claims 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumagi (US 5,397,906) in view of Nagakubo et al. (US 4,478,655) as applied to claims 34, 35, and 38 above, and further in view of Yatsuda et al (US 4,668,970).

In re claim 41, Kumagi and Nagakubo show all of the elements of the claims except the second insulating film having a plurality of insulating films stacked. Yatsuda et al. shows (fig. 4b) an isolation region (7) being a multilayered insulating film having a plurality of insulating films (7, 40, 5, 40') stacked. A field shield electrode (5) is formed on the isolation film to provide a tunable isolation region. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the isolation region of Kumagi and Nagakubo by forming a multilayered insulation film as taught by Yatsuda to provide adequate isolation for a semiconductor active region.

In re claims 42-44, the limitations of the claims pertain to "product by process." See the explanation above concerning "product by process" limitations.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Waggoner (US 5,420,447) and Tanaka et al. (US 5,331,181) also show semiconductor devices having isolated gate arrays or isolation regions having multiple layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GEORGE ECKERT
PRIMARY EXAMINER

MEW
MEW
January 24, 2005